-- This application is a divisional of U.S. Patent Application S/N 08/890,341 filed 10 Jul 1997 by Howard T. Olnowich for Memory Controller for Controlling Memory Accesses Across Networks in Distributed Shared Memory Processing Systems (as amended), now U. S. Patent 6,044,438 issued 28 March 2000, other divisions of which have issued on 19 Sep 2000 as U. S. Patents 6,122,659 and 6,122,674.--

Please replace the paragraph beginning at line 4 of page 1 with the following rewritten paragraph:

-- U.S. patent application Serial No. 08/891,404, filed 10 Jul 1997, entitled "Cache Coherent Network Adapter for Scalable Shared Memory Processing Systems", (now U.S. patent 6,092,155 issued 18 Jul 2000 and pending divisional application S/N 09/516,393 filed 1 Mar 2000) filed concurrently herewith is assigned to the same assignee hereof and contains subject matter related, in certain respects, to the subject matter of the present application; it is incorporated herein by reference.--

Please replace the paragraph beginning at page 12, line 2, with the following rewritten paragraph: